Determining FPGA capabilities for CubeSat lidar constellation

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Objective:
Demonstrate the capabilities of a Field Programmable Gate Array (FPGA) board to meet the needs of a multistatic space lidar constellation, including self-monitoring, processing data, and generating outputs.

BACKGROUND

Cube satellites (CubeSats) have recently become a popular tool to provide affordable access to space for the scientific community[1]. The Navy can utilize CubeSats to gather invaluable information about the planet in an affordable manner. Rainbow, a multistatic space lidar constellation mission, is starting its phase A in August 2018 and will supply critical information about the battlespace environment. In order to increase the Technical Readiness Level (TRL) of lidar hardware so it is suitable for miniaturization and application in a hostile environment, I performed preliminary studies to determine the capabilities of a System on a Chip (SoC) FPGA suitable for such applications.

Fig. 1 Example CubeSat

CUBESAT OVERVIEW

The electronic systems of Rainbow will perform a variety of functions critical for both the platform and the instrument. For the lidar receiver, they include sending transistor-transistor logic (TTL) signals to the photomultiplier tubes synchronized with the laser shot, taking in data, processing and storing the data, and self-monitoring. A sufficient CPU load margin is important to ensure that a minor anomaly will not cause a catastrophic failure of the satellite.

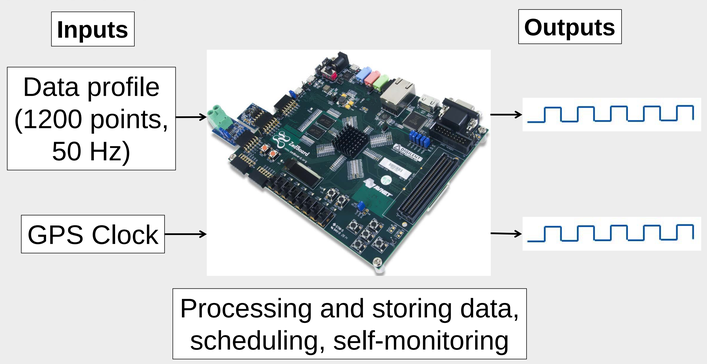

Fig. 2 Concept of CubeSat receiver's functions

Since one of the possible platforms for Rainbow utilizes the Xilinx Zynq 7020 chip, I focused my electronic studies on the ZedBoard, an evaluation and development board that uses Zynq. As an FPGA, this board allows for user hardware modifications and stores the configuration within its memory, giving users the ability to easily specialize their processor. As such, I designed the ZedBoard to function as a computer, with an operating system (OS) and various input/output (I/O) ports.

METHOD

I took the bare metal application and loaded PetaLinux onto the flash memory, providing basic Linux commands onto the embedded system. I then rebuilt the Linux kernel to add a C compiler (GCC) to PetaLinux, eliminating the need for cross-compiling. To incorporate the various I/O and sensors on the FPGA as Programmable Logic (PL), I rewrote the Hardware Description Language (HDL) to include multiple General Purpose I/O's (GPIOs), Peripheral Modules (Pmods), and an Analog Mixed Signal (AMS) Evaluation Card. I then exported a board support package which allows the software to access the new hardware.

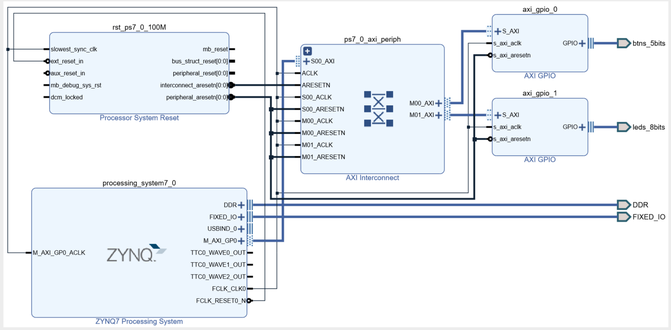

Fig. 3 Writing HDL in Vivado

The GPIOs allowed me to interface with the onboard LEDs as well as send TTL signals. The Pmod Inertial Measurement Unit (IMU) supplied me with a variety of orientation related data. The AMS Card provided simple system monitoring for internal temperature and power. Lastly, the Pmod Analog/Digital Converter (ADC) showed the board's capacity to convert the analog signals from a photomultiplier (PMT) to provide data profiles to the CubeSat.

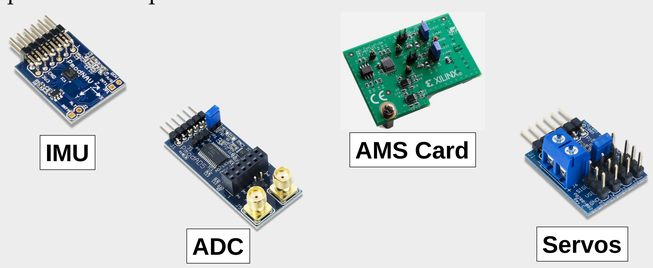

Fig. 4 External Components used[2] [3]

REFERENCES

[1]https://www.nasa.gov/sites/default/files/atoms/files/nasa_csli_cubesat_101_508.pdf
[2]https://store.digilentinc.com/
[3]https://www.xilinx.com/products/boards-and-kits/hw-ams101-g.html

RESULTS

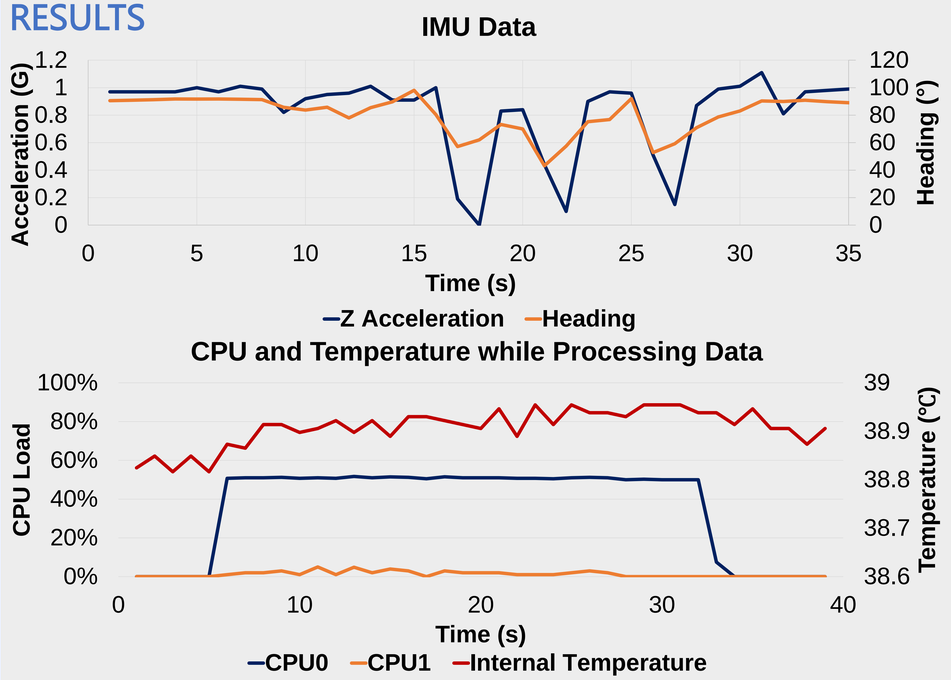

Fig. 5 Simulations of Zedboard's capabilities

My modifications have enhanced our understanding of the chip's capabilities as compared to before. To simulate the board's performance during operation, I ran multiple tests that demonstrated the Pmods' various capacities. To test the CPU load and internal temperature of the dual-core processors, I ran a simple code to average five million data points and observed its effect on the CPU.

CONCLUSION

The Rainbow mission will produce the first CubeSat lidar and first space lidar constellation. To ensure that the electronic chips onboard the CubeSats will have the capabilities needed to receive and transmit data as well as self-monitor their systems, various tests were performed to increase the TRL of this SoC. The results so far are favorable to consider this technology for the space lidar constellation. The FPGA demonstrates the desired capabilities for the lidar receiver. In the future, we will integrate synchronization/scheduling and test remote modifications of the implemented algorithm.

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